Docket No.: 57454-990 <u>PATENT</u>

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 20277

Hideyuki NODA, et al. : Confirmation Number: To be assigned

Serial No.: Continuation of : Group Art Unit: To be assigned

Application No. 09/632,333

Filed: November 17, 2003 : Examiner: To be assigned

For: LOGIC-MERGED MEMORY

INFORMATION DISCLOSURE STATEMENT

Mail Stop NEW APPLICATION Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

The references were cited by or submitted to the U.S. Patent and Trademark Office in parent application Serial No. 09/632,333, filed August 3, 2000, which is relied upon for an

Serial No.: Continuation of

Application No. 09/632,333

earlier filing date under 35 USC 120. Thus, copies of these references are not attached. 37 CFR

1.98(d).

Please charge any shortage in fees due in connection with the filing of this paper, including

extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit

account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Stephen A. Becker

Registration No. 26,527

600 13th Street, N.W.

Washington, DC 20005-3096 (202) 756-8000 SAB:BD

Facsimile: (202) 756-8087

Date: November 17, 2003

INFORMATION DISCLOSURE CITATION IN AN APPLICATION				ATTY. DOCKET NO. 57454-990		SERIAL NO. Continuation of S rial No. 09/632,333	
			APPLICANT Hid yuki NODA, et al.				
(PTO-1449)				FILING DATE November 17, 2003		GROUP To be assigned	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	PATENT NO. ATE		NAME		SUBCLASS	FILING DATE
	5,101,248	101,248 3/31/1992		TAKEBUCHI			
	5,293,336	3/8/1994	Ishii et al				
	5,825,712	10/20/98	Higashi et	al			
	4,482,985	11/13/84	Itoh et al				
	4,471,373	9/1984	Shimizu et al				
	5,610,858	3/1997	Iwahashi				
	5,256,892	10/93	Yoshida				
	2001/0010654	8/2001	Shau				
	5,592,434	1/1997	Iwamoto e	t al			
				-			
FOREIGN PATENT DOCUMENTS							
EXAMINER'S NITIALS	PATENT NO.	DATE	OI	JNTRY	CASS	SUBCASS	Transation
			~~	OOMA		SOBCASS	Yes
			JAPAN (with abstract)	APAN (with English ostract)			
	11-214656A			apan (Shimizu et al)			
				,			
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
"A 5.3-GB/s Embedded SDRAM Core with Slight-Boost Scheme", A. Yamazaki et al., IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 34, NO. 5, MAY 1999, pp. 661-667							
EXAMINER DATE CONSIDERED							